



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,699	12/18/2001	Chi-Keung Luk	200302 184-1 (1662-46800)	3236
22879	7590	01/18/2006	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			TO, JENNIFER N	
			ART UNIT	PAPER NUMBER
			2195	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,699	LUK ET AL.	
	Examiner	Art Unit	
	Jennifer N. To	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-36 are pending for examination.
2. Examiner does not consider the two Non-Patent-Literatures enclosed with Applicant's Arguments/Remarks filed on 09/19/2005. Applicant needs to list these Non-Patent-Literatures in an appropriated PTO1449 form for examiner to be considered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter in which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. As per claims 1, 10, and 19, the amended claims recited the amended limitation "only a portion, but not all". However, the limitation "only a portion, but not all" is not supported by the specification. For example, it is noted that in applicants' specification, page 1, 3rd paragraph, line 4, and page 3, 8th paragraph, line 3, disclosed "at least a portion". Nowhere in the specification support the amended limitation. Therefore, these

amended claims contain subject matter in which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg (AR-SMT: A Microarchitectural Approach to fault Tolerance in Microprocessors), and in view of Georgiou et al. (hereafter Georgiou) (U.S. Patent No. 6032245).

8. Rotenberg was cited in the previous office action.

9. As per claim 1, Rotenberg teaches the invention substantially as claim including a computer system (fig. 1), comprising:

a main system memory coupled to said processor (memory where program p is stored; fig. 1B; page 2, right column, line 52);

wherein said processor processes a program in a main thread that includes instructions which cause the processor to spawn a pre-execution thread, said pre-execution thread runs concurrently with the main thread, but ahead of the main thread in program order (figs. 1B, 3; page 2, right column, lines 45-46, left column, lines 28-29; page 3, right column, lines 7-10).

Rotenberg did not specifically teach that at least a portion of the same program executes.

10. However, Georgiou teaches that at least a portion of the same program executes (fig. 1; col. 2, lines 65-67; col. 3, lines 1-7).

11. It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have combined the teaching of Rotenberg and Georgiou because Georgiou teaching that at least a portion of the same program executes would improve the integrity of Rotenberg by increasing the amount of parallel execution in the system (Georgiou, col. 2, lines 36-37).

12. As per claim 2, Rotenberg teaches that wherein said instructions that cause the pre-execution thread to be spawned include a start instruction which causes a pre-execution thread to start and a stop instruction which causes the pre-execution thread to stop (fig. 3A).

13. As per claim 3, Rotenberg teaches that wherein said start instruction includes a value designating the location in the program where the pre-execution thread is to start running (fig. 3A).

14. As per claim 4, Rotenberg teaches that wherein the pre-execution thread encounters a cache miss condition for a memory reference but the main thread does not encounter a cache miss condition when that same memory reference is processed by the main thread (page 5, right column, lines 1-14).

15. As per claim 5, Rotenberg teaches that wherein said processor determines whether sufficient hardware resources are available before spawning said pre-execution thread. (page 2, left column, lines 28-31).

16. As per claim 6, Rotenberg teaches that wherein said processor ignores exception conditions generated during the pre-execution thread (page 6, right column, lines 22-27).

17. As per claim 7, Rotenberg teaches that wherein said processor does not permit a store instruction in the pre-execution thread to modify main system memory contents (page 2, left column, lines 45-52).

18. As per claim 8, Rotenberg teaches that wherein said processor does not permit any store instruction in the pre-execution thread to modify main system memory contents (page 2, left column, lines 45-52).

19. As per claim 9, Rotenberg further teaches the step of including a buffer into which pre-execution thread stores data is written to make such store data available to pre-execution thread load instructions (page 2, right column, lines 45-52).

20. As per claim 10, it is rejected for the same reason as claim 1 above. In addition, Rotenberg teaches the processor comprising:

- a fetch unit capable of fetching instructions from a plurality of threads (page 3, right column, line 2);

- a program counter coupled to said fetch unit (page 5, right column, lines 15-16);

- an instruction cache coupled to said fetch unit (fig. 5, trace cache);

- a data cache coupled to said instruction cache (fig. 5, fetch, dispatch, issue execute D-cache).

21. As per claims 11-18, they are rejected for the same reason as claims 2-9 above.

22. As per claim 19, it is rejected for the same reason as claims 1, and 10 above. In addition, Rotenberg teaches the step of inserting instructions to generate a pre-execution thread in a processor into a program:

inserting pre-execution thread instructions in the program (figs. 1B, 3A);
spawning a pre-execution thread when designated by the inserted instruction (fig. 1B instr i'); and
running said pre-execution thread concurrently with a main thread wherein both the pre-execution and the main threads include instructions from the same program, the pre-execution thread running ahead of the main thread (figs. 1B, 3; page 2, left column, lines 28-29; page 3, right column, lines 7-10).

23. As per claims 20, 22-24, and 26-30, they are rejected for the same reason as claims 2-3, and 5-9 above.

24. As per claim 21, Rotenberg teaches copying register contents associated with the main thread to registers used by the pre-execution thread (page 5, left column, lines 34-37).

25. As per claim 25, Rotenberg teaches copying the contents of at least one register to memory to make such contents available to the pre-execution thread (page 5, left column, lines 34-37).

26. As per claims 31-32, they are rejected for the same reason as claims 1, and 10 above. In addition, Georgiou teaches that wherein, in a pre-execution thread, said

processor pre-executes instructions from a main thread that are specified by said main thread (col. 2, lines 20-47).

27. As per claim 33, Rotenberg teaches a pre-execution thread spins on a variable that is set to a predetermined value by the main thread when there are instructions to pre-execute (fig. 3A).

28. As per claim 34, Rotenberg teaches the processor ceases pre-executing instructions when a program counter is encountered that exceeds a range (page 6, left column, lines 34-38).

29. As per claim 35, Rotenberg teaches the processor ceases pre-executing instructions when the main thread catches up to the pre-executing instructions (page 6, left column, lines 24-26).

30. As per claim 36, Rotenberg teaches the processor ceases pre-executing instructions when the number of pre-executing instructions exceeds a limit (page 6, left column, lines 23-24).

Response to Arguments

31. Applicant's arguments with respect to claims 1, 10, 19, and 31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chintalapati et al. (U.S. Patent No. 6457063) teaches monitoring daemon processes.

Johnston et al. (U.S. Patent No. 5781776) teaches permitting program editing during program execution.

Cox et al. (U.S. patent No. 6199117) teaches generalized control for starting of tasks.

Khan et al. (U.S. patent No. 6219782) teaches multiple user software debugging system.

Strout et al. (U.S. Patent No. 5339415) teaches dual level scheduling of processes to multiple parallel regions of a multi-threaded program.

Mohamed et al. (U.S. patent No. 5978838) teaches coordination and synchronization of an asymmetric, dual multiprocessor.

Saxon (U.S. Patent No. 5261097) teaches method for executing command scripts using multiple synchronized threads.

Chastain et al. (U.S. Patent No. 5159686) teaches multi-processor computer system having process-independent communication register addressing.

Motomura (U.S. Patent No. 5815727) teaches parallel processor for executing plural thread program.

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer N. To whose telephone number is (571) 272-7212. The examiner can normally be reached on M-T 6AM- 3:30 PM, F 6AM- 2:30 PM.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.


Art Unit: 2195

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer N To
Examiner
Art Unit 2195


MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2195